AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1003] with the following amended paragraph:

[1003] A common method of performing the initial VCO calibration is discussed with reference to Prior Art Figs. 1-3. A set of quadrature clocks CLK0, and CLK90 are generated using a VCO. One of the quadrature clocks CLK0, sometimes referred to herein as the "recovered clock," is a copy of the VCO's output, and the other quadrature clock CLK90 is a 90 degree phase shifted version of the first clock CLK0. Data transitions 105, 107, and 109 are each assigned to one of four quadrants Q1, Q2, Q3, or Q4 based on the state (either high or low) of both CLK0 and CLK90. For example, data transition 105 occurs at time 110, when CLK0 is high and ~~CLK 90~~ CLK90 is low. Consequently data transition 105 is assigned to quadrant Q1. Similarly, data transition 107 occurs at time 120, when both CLK0 and CLK90 are low, and is assigned to quadrant Q4. Data transition 109, which occurs at ~~time 130~~ time 135 when CLK0 is low and CLK90 is high, is assigned to quadrant Q3. Although not illustrated, a data transition that occurs when both CLK0 and ~~CLK 90~~ CLK90 are high is assigned to quadrant Q2.

Please replace paragraph [1014] with the following amended paragraph:

[1014] Various embodiments of the present invention also include a transition density counter. If the transition density counter determines that there is an insufficient number of transitions to ~~insure~~ ensure an accurate frequency determination, the frequency detector sets a transition density output to indicate [[to]] that no frequency adjustments should be made to the VCO, regardless of whether the frequency adjustment signals so indicate.

Please replace paragraph [1034] with the following amended paragraph:

[1034] The three outputs of each frequency detector 440-470 are connected to the inputs of VCO control 410. VCO control 410 combines the outputs of all four frequency detectors 440-470, applies control parameters, as subsequently discussed, and provides a control signal to DAC 420. DAC 420 converts the digital control signal provided by VCO 410 into an analog signal suitable for controlling the voltage controlled oscillator 430. The control signal provided by DAC 420 causes the frequency of VCO 430 to be adjusted to an average frequency of all four data channels, and the output of VCO 430 is then fed back to frequency detectors 440-470, where the new frequency is compared to the frequency of each data channel, and the cycle repeats.

Please replace paragraph [1036] with the following amended paragraph:

[1036] Referring next to Figs. 5-7, the frequency detector and some of its sub-components will be discussed according to an embodiment of the present invention. Fig. 5 illustrates filter 505 and direction detector 530 according to an embodiment of the present invention. Inputs received at frequency detectors 440-470 ~~(Fig. 1)~~ (Fig. 4) are received in each of the frequency detectors at filter 505. A quadrant shift register 510 receives the recovered clock ~~CLK 0~~ CLK0 and shifted recovered clock ~~CLK 90~~ CLK90, and is clocked by data transmissions from data channel DIN. In the illustrated embodiment, quadrant shift register 510 is capable of holding information related to eight transitions of data stream DIN. Other embodiments may be implemented, however, wherein quadrant shift register 510 is configured to hold more or fewer than eight data transitions.

Please replace paragraph [1037] with the following amended paragraph:

[1037] The output of quadrant shift register 510 is connected to selector 520, and provides the quadrant information associated with each data transition to selector 520. Selector 520 chooses which of the quadrant information associated with the data transitions are to be provided to direction detector 530 for a comparison. Selector 520 provides quadrant information for a first selected data transition over Qold to direction detector 530, and delivers quadrant information associated with a second selected data transition over line Qnew. Direction detector 530 compares the quadrant information for the first selected data transition and the second selected data transition to determine a frequency relationship between the VCO 430 ~~(fig. 4)~~ (Fig. 4) and the data stream. Once direction detector 530 determines, based on the quadrant information of the selected data transitions, whether the data frequency is faster or slower than the VCO frequency, direction detector 530 generates an increase signal, a decrease signal, or neither, indicating the appropriate direction in which to adjust the frequency of the VCO to match the frequency of the data stream.

Please replace paragraph [1038] with the following amended paragraph:

[1038] Referring next to Fig. 7, two counters, 702 and 704, are illustrated. The increase and decrease signals generated by direction detector 530 are provided to counters 702 and 704. Both counters 702 and 704 count the number of increase and decrease signals generated by direction detector 530 whenever the corresponding enable signals ~~COUNT 0, COUNT 1~~ COUNT0, COUNT1, are active. Counter 702 includes ripple counter 705 and ripple counter

710, while counter 704 includes ripple counter 715 and ripple counter 720. The operation of both counters, 702 and 704, are analogous. Two counters are used in one embodiment to provide a staggered, overlapping count window so that no transitions are missed. Ripple ~~counter~~ counters 705 and 715 count the number of increase frequency signals generated by direction detector 530, and ripple counters 710 and 720 count the number of decrease signals generated by direction detector 530. The output of ripple counter 705 FINC0 and the output of ripple counter 715 FINC1 are provided to VCO control 410 (Fig. 4) to indicate that the frequency of VCO 430 should be increased. The output of ripple counters 710 FDEC0, and the output of ripple counter 720 FDEC1, are provided to VCO controller 410 (Fig. 4) to indicate that the frequency of VCO 430 should be decreased.

Please replace paragraph [1039] with the following amended paragraph:

[1039] Referring next to Fig. 6, ripple counters 605 and 607 are illustrated, and serve the purpose of transition density counters in one embodiment of the present invention. Like ~~counter~~ counters 702 and 704, the transition density ripple counters 605 and 607 are used to provide staggered, overlapping count windows. Ripple ~~counter~~ counters 605 and 607 may be configured to count each data transition of data channel DIN. The outputs of ripple counters 605 and 607, TD0 and TD1, respectively, are provided to VCO control 410 (Fig. 4) to indicate whether sufficient data transitions are present in the data stream DIN to allow an accurate frequency determination.

Please replace paragraph [1042] with the following amended paragraph:

[1042] In one embodiment, when selector 520 is set to select data transitions delayed by 1, the quadrant of each data transition is compared to the quadrant of each immediately preceding data transition. So, e.g., direction detector 530 compares data transition B with first data transition A, data transition C with data transition B, etc. The result of comparing data transition B with data transition A is 0, because both data transitions A and B are assigned to quadrant 1. When direction detector 530 compares data transition E to data transition D, the result is indeterminate, because data transitions D and E occur in opposing quadrants, and may indicate either that the frequency of the voltage control oscillator needs to be increased or decreased. When direction detector 530 compares data transition F to data transition E, the result is negative, indicating that the frequency of the VCO should be decreased to match the frequency of the data channel. A comparison of data transition I (quadrant 3) with data transition H

(quadrant 2) gives a result which is positive, and indicates that the frequency of the VCO should be increased to match the frequency of the data channel.

Please replace paragraph [1043] with the following amended paragraph:

[1043] In at least [[on]] one embodiment, selector 520 varies the delay between selected data transitions so that, during particular intervals, quadrant information for data transitions delayed by either one delay, two delays, four delays or eight delays is used. In the case of two transition delays shown in the "2 Transitions" row of Fig. 8, selector 520 selects quadrant information from every other data transition for delivery to detector 530. For example, selector 520 might provide data transition C over line Qold (Fig. 5) and data transition E over line Qnew (Fig. 5). The result of the comparison in this example would be indeterminate, because data transitions E and C occur during opposing quadrants.

Please replace paragraph [1044] with the following amended paragraph:

[1044] During a time in which selector 520 is using two delays as its selection criteria, selector 520 may also provide data transition G and E to direction detector 530 for comparison. In such a case, the result indicates that the frequency of the VCO should be reduced to match the frequency of the data channel, since transition G occurs in quadrant 2 and transition E occurs in quadrant 3. Similarly, a comparison of data transition I (quadrant 3) and data transition [[851]] G (quadrant 2) yields a result indicating that the frequency of the VCO should be increased to match the frequency of the data channel.

Please replace paragraph [1047] with the following amended paragraph:

[1047] Referring next to ~~Figs 6,~~ Figs. 6, 7 and 9, staggered overlapping count windows will be discussed. At 905, bank 0, which corresponds to ripple counter 605 in Fig. 6 and counter 702 in Fig. 7, ~~begin~~ begins to count. At 910, bank 1, which corresponds to ripple counter 607 in Fig. 6 and counter 704 in Fig. 7, is held. At 915, bank 1 is latched, so that the data held in bank 1 can be delivered to VCO control 410 (Fig. 4). At 920, bank 1 is cleared, and at 925, bank 1 begins to count. After bank 1 begins to count in 925, bank 0 is held at 930. At 935, bank 0 is latched and at 940, bank 0 is cleared. If the trial counter TC indicates that a particular trial has completed, then after bank 0 is cleared at 940, the trial number is incremented at 945. If, however, the current trial has not finished yet, after bank 0 is cleared, bank 0 begins counting again.

Please replace paragraph [1050] with the following amended paragraph:

[1050] Referring next to Fig. 10, different ~~trails~~ trials through which VCO control 410 cycles are discussed according to an embodiment of the present invention. Each trial, or control state, corresponds to particular settings of gain, filter delay and dither. During trial 1, the gain of the frequency-locked loop is set to 1, the filter delay of selector 520 (Fig. 5) is set to use one delay, and a random or pseudo random amount of dither corresponding to .112 % RMS is induced into the VCO 430 (Fig. 4) to compensate for possible low gain in the data channel. During trial 2, the gain is set to ½, the filter is set to implement two delays, and the dither is set to .028 % RMS. During trial 3, the gain is set to ¼, the filter is set to four delays, and the dither is set to .007 % RMS. Finally, during ~~trail~~ trial 4, the gain is set to 1/8, the filter delay is set to eight and no dither is added. Note that as the trials progress from 1 to 4, the filter delay increases from one delay to eight delays. Note that the delay is implemented gradually, starting with only one delay and progressing to eight delays, to prevent the filter 505 from providing false outputs if the frequency error is too high. Applying the delay gradually allows the frequency error to diminish between settings.

Please replace paragraph [1052] with the following amended paragraph:

[1052] Referring next to Fig. 12, a loss of lock calculation is discussed according to an embodiment of the present invention. Recall that for the illustrated embodiments there are four channels and eight stages of filtering in quadrant shift registers 510 (Fig.5). The number of counts = $4 * 8 * Kf * T_{int} * \Delta f$. The finite state machine illustrated in Fig. 9, which ~~effects~~ affects both the transition density and the frequency adjustments is, in this example, operated by a divide by 32 clock. Therefore, $Kf = 4 * (7/5)$, $f_{err} = \Delta f / f_{nom}$ and $T_{int} = N * 32 / f_{nom}$. Therefore, counts = $4 * 8 * 4 * (7/5) * 32 * N * f_{err}$. With N = 8192, $K_{lol} = 256$ and target =92, $f_{err} = (92 * 256) / 4 / 8 / 4 / (7/5) / 32 / 8192 = 0.05$ %.

Please replace paragraph [1055] with the following amended paragraph:

[1055] VCO control 410 sums the net counts, or zeros, from all four data channels (FD_Sum_TR) to produce FD_Sum. VCO control 410 applies a gain to FD_Sum based on the current trial in which VCO control 410 is operating. Note that in one embodiment, a gain based on the frequency adjustment signals from the frequency detectors (FD_Gain) is first applied, and then decreased according to the current trial.

Please replace paragraph [1056] with the following amended paragraph:

[1056] A pseudo random bit is generated, [[an]] and a gain is applied at FD_PRBS_Gain. The pseudo random bit will be either a 0 or a 1, so that either some amount of dither (determined by the gain applied and the particular trial in which VCO control 410 is operating) will be supplied, or no dither at all will be added. Any dither is added to the adjustment to generate a composite FD_Sum _Shift signal which is then provided to DAC 420 for control of VCO 430.

Please replace paragraph [1057] with the following amended paragraph:

[1057] Referring next to Fig. 14, a data path for a loss of lock (LOL) indicator is discussed according to an embodiment of the present invention. The signal FD_Sum, which is the same signal FD_Sum illustrated in Fig. 13, is compared to a loss of lock target value LOL_TARGET. Recalling that FD_Sum may indicate either a number of frequency increase signals or a number of frequency decrease signals, both a positive and negative loss of lock differential signal are generated. The positive loss of lock differential signal LOL_DIFF_POS is used to determine if the number of frequency increases has exceeded the target value LOL_TARGET. Likewise, the negative differential signal LOL_DIFF_NEG is used to determine whether the number of frequency decrease signals exceeds the target value. If either LOL_DIFF_POS or LOL_DIFF_NEG are less than zero, a loss of lock signal LOL is generated.

Please replace paragraph [1058] with the following amended paragraph:

[1058] Although various embodiments of the present invention have been shown and described [[at]] in detail herein, many other varied embodiments of the present invention may be practiced without departing form the teachings set forth herein. These embodiments can be readily constructed by those skilled in the art. Accordingly, the present invention is not intended to be limited to the specific forms set forth herein, but to the contrary, includes such alternatives, modifications, and equivalents as can be reasonably included within the spirit and scope of the invention.